

## P-Channel MOSFET MEM2309S

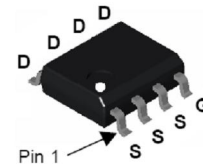
### Description :

MEM2309SGSeries P-channel enhancement mode field-effect transistor ,produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance.

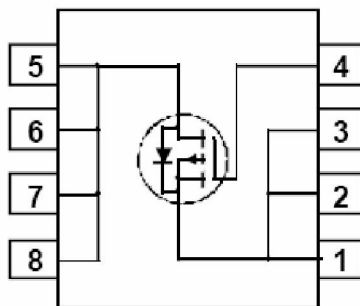
This device particularly suits low voltage applications, and low power dissipation.

### Feature :

- | -30V/-6A  
 $R_{DS(ON)} = 53m @ V_{GS} = -10V, I_D = -6A$
- |  $R_{DS(ON)} = 68m @ V_{GS} = -4.5V, I_D = -4A$
- | High Density Cell Design For Ultra Low On-Resistance
- | Surface mount package:SOP8



### Pin Configuration :



### Typical Application:

- | Power management
- | Load switch
- | Battery protection

### Absolute Maximum Ratings:

Parameter	Symbol	Ratings	Unit	
Drain-Source Voltage	$V_{DSS}$	-30V	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V	
Drain Current	$I_D$	$T_A = 25$	-6	A
		$T_A = 70$	-3.2	
Pulsed Drain Current <sup>1,2</sup>	$I_{DM}$	-30	A	
Total Power Dissipation	$P_d$	$T_A = 25$	2	W
		$T_A = 70$	0.8	
Operating Temperature Range	$T_{Opr}$	150		
Storage Temperature Range	$T_{stg}$	-65/150		

## Thermal Characteristics:

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Ambient <sup>3</sup>	R JA	50	/W

## Electrical Characteristics:

### MEM2309SG

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-34		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.1	-1.3	-2	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=20V$		5	30	nA
		$V_{DS}=0V, V_{GS}=-20V$		-5	-30	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$		-6	-300	nA
Static Drain-Source On-Resistance	$R_{DS(ON)1}$	$V_{GS}=-10V, I_D=-6A$	33	53	65	m
	$R_{DS(ON)2}$	$V_{GS}=-4.5V, I_D=-4A$	50	68	80	m
Forward Transconductance	$g_{FS}$	$V_{DS} = -5 V, I_D = -5.3 A$		10		S
Drain-Source Diode Forward Current	$I_S$				-2.1	A
Source-drain (diode forward) voltage	$V_{SD}$	$V_{GS}=0V, I_D=-1A$		-0.8	-1.2	V
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0 V, f = 1 MHz$		530		pF
Output Capacitance	$C_{oss}$			140		
Reverse Transfer Capacitance	$C_{rss}$			70		
<b>Switching Characteristics</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 V, I_D=-1 A, V_{GEN} = -10 V, R_g = 6$		8	15	ns
Rise Time	$t_r$			15	25	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall-Time	$t_f$			10	15	
Total Gate Charge	$Q_g$	$V_{DS} = -15 V, V_{GS} = -10 V, I_D = -4A$		10	15	nC
Gate-Source Charge	$Q_{gs}$			2.2		
Gate-Drain Charge	$Q_{gd}$			2.0		

- 1、Repetitive rating, pulse width limited by junction temperature.
- 2、Pulse test; pulse width 300 us, duty cycle 2%.
- 3、Surface Mounted on FR4 Board, t 10 sec.

## Typical Performance Characteristics :

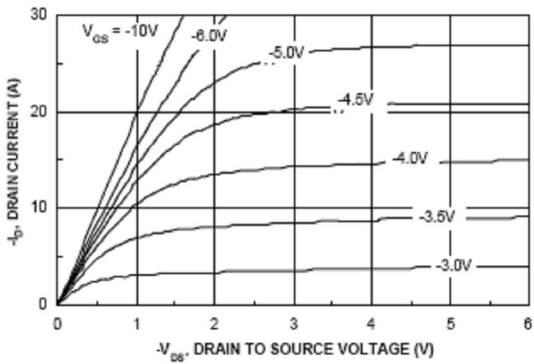


Figure 1. On-Region Characteristics.

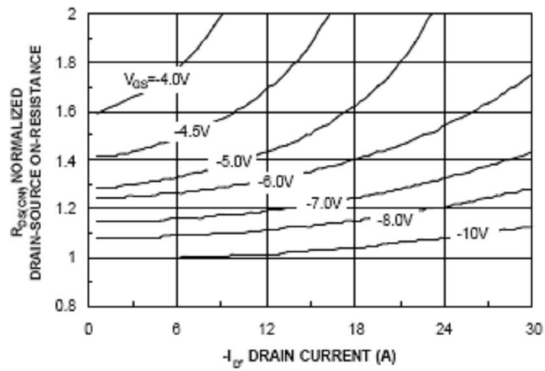


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

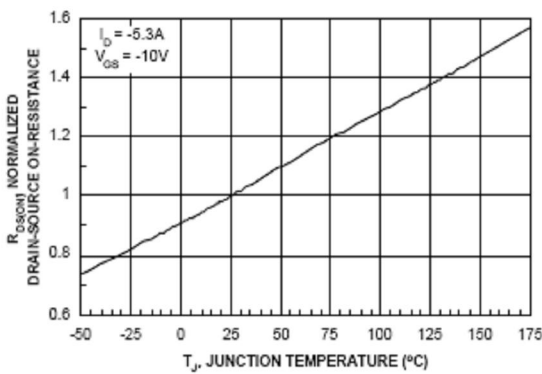


Figure 3. On-Resistance Variation with Temperature.

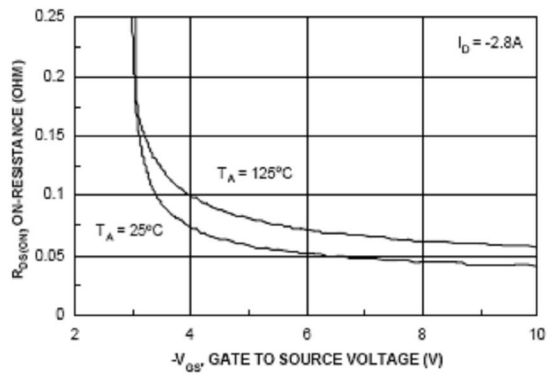


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

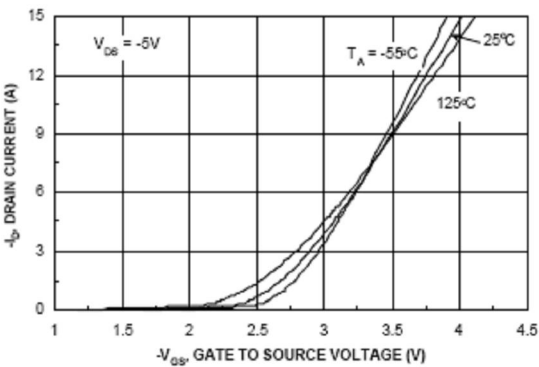


Figure 5. Transfer Characteristics.

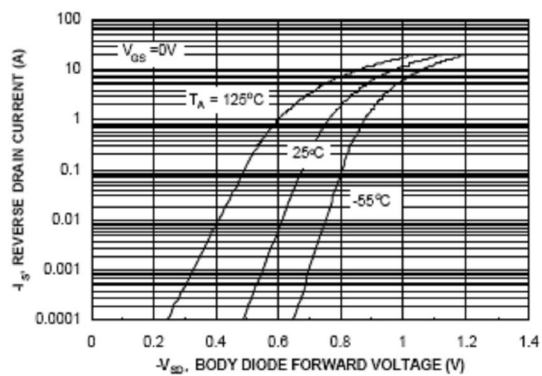
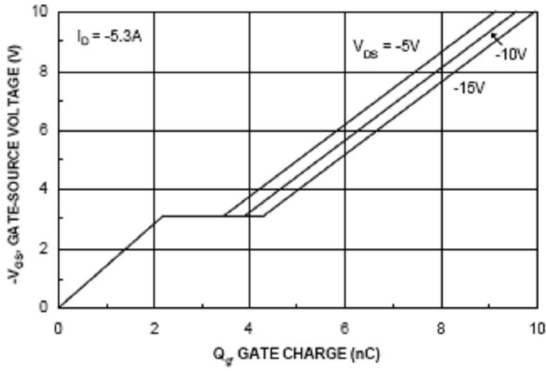
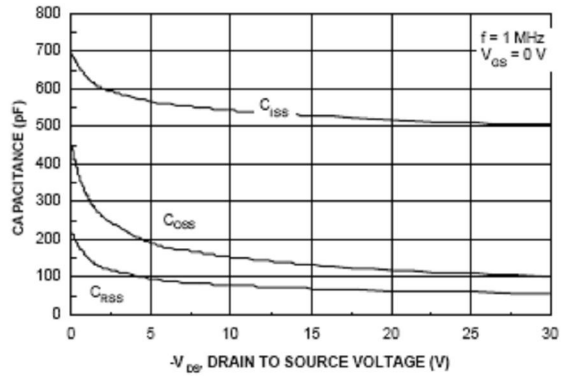


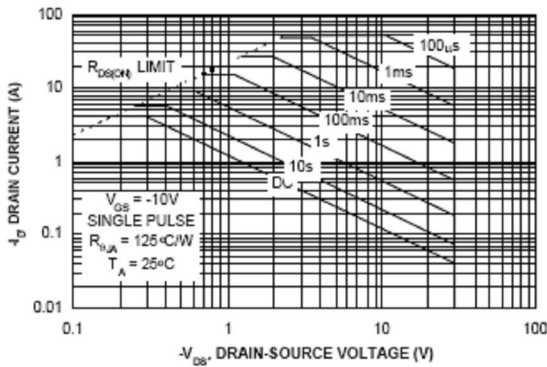
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



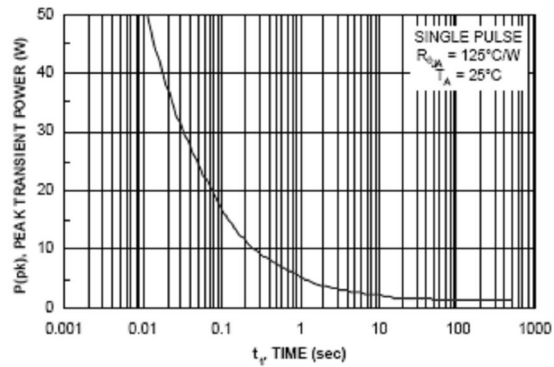
**Figure 7. Gate Charge Characteristics.**



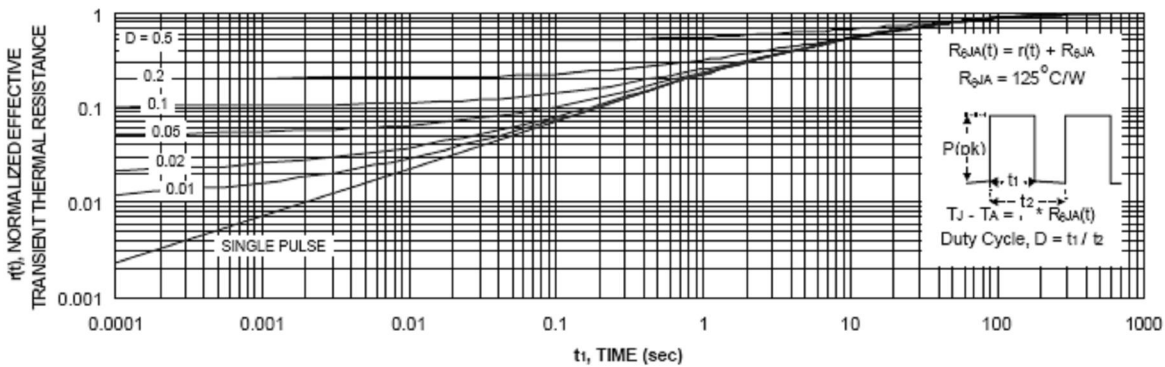
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



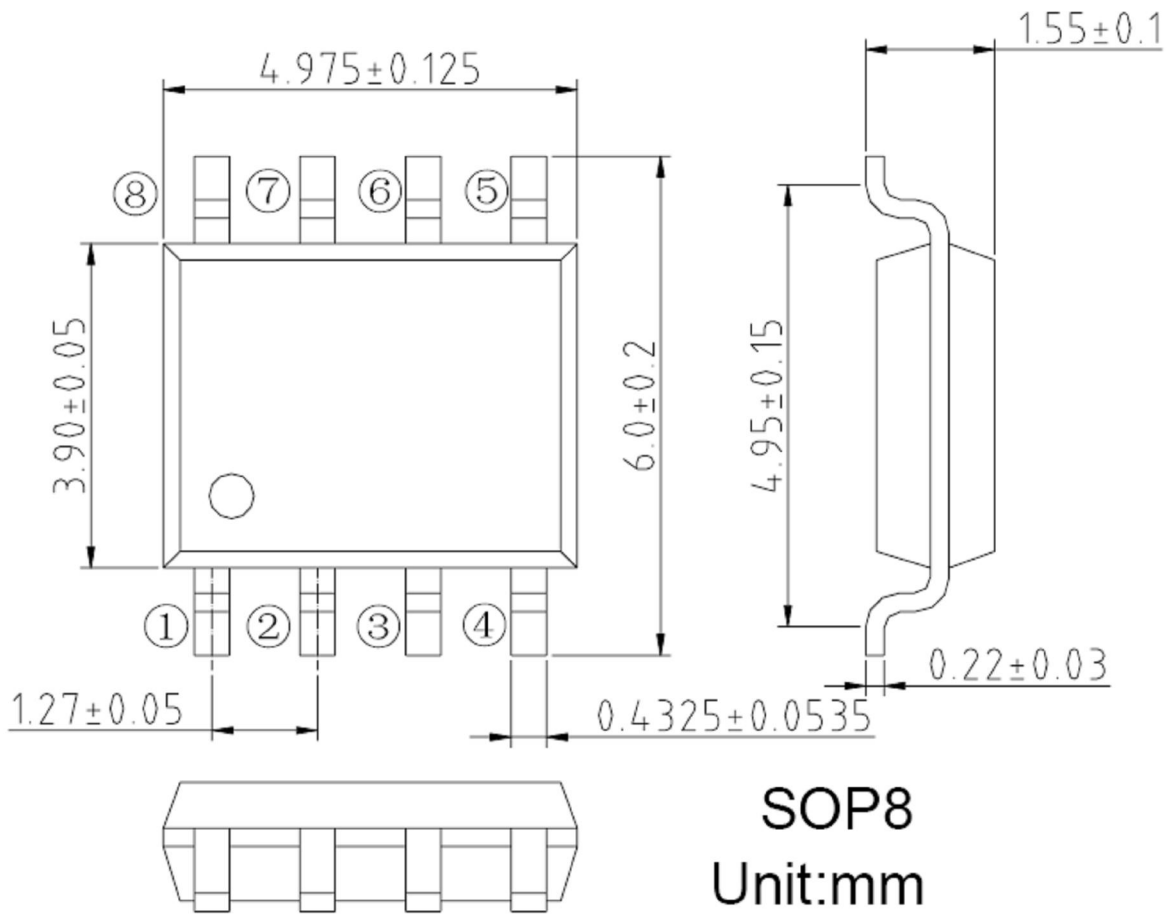
**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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