

## N-Channel MOSFET MEM8205F

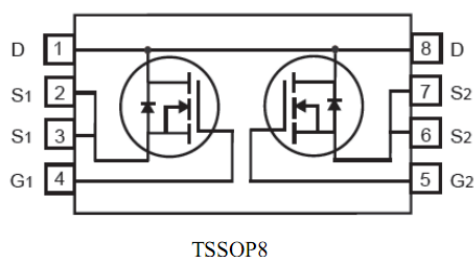
### General Description

MEM8205FG Dual N-channel enhancement mode field-effect transistor, produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation.

### Features

- 20V/6A  
 $R_{DS(ON)} = 20m\Omega @ V_{GS}=4.5V, I_D=6A$   
 $R_{DS(ON)} = 21m\Omega @ V_{GS}=3.85V, I_D=5A$   
 $R_{DS(ON)} = 26m\Omega @ V_{GS}=2.5V, I_D=4A$
- High Density Cell Design For Ultra Low On-Resistance
- Surface mount package:TSSOP8

### Pin Configuration



### Typical Application

- Battery management
- Power management
- Portable equipment
- Low power DC to DC converter.
- Load switch
- LCD adapter

### Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		$V_{DSS}$	20V	V
Gate-Source Voltage		$V_{GSS}$	$\pm 12$	V
Drain Current	$T_A=25^\circ C$	$I_D$	6	A
Pulsed Drain Current <sup>1,2</sup>		$I_{DM}$	20	A
Total Power Dissipation	SOT23-6	$P_d$	1.25	W
	TSSOP8		1.5	
operating junction temperature		$T_j$	150	$^\circ C$
Storage Temperature Range		$T_{stg}$	-65/150	$^\circ C$

## Thermal Characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Ambient <sup>3</sup>	R $\theta$ JA	100	°C/W

## Electrical Characteristics

MEM8205FG

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	21.5		V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.5	0.66	1	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =12V			100	nA
		V <sub>DS</sub> =0V, V <sub>GS</sub> =-12V			-100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =16V V <sub>GS</sub> =0V		2.5	1000	nA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		20	24	mΩ
		V <sub>GS</sub> =3.85V, I <sub>D</sub> =5A		21	25	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4A		26	35	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 4.5A		10		S
Drain-Source Diode Forward Current	I <sub>S</sub>				1.7	A
Source-drain (diode forward) voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =1.25A		0.8	1.0	V
<b>Dynamic Characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V, f = 1 MHz		600		pF
Output Capacitance	C <sub>oss</sub>			330		
Reverse Transfer Capacitance	C <sub>rss</sub>			140		
<b>Switching Characteristics</b>						
Turn-On Delay Time	td(on)	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> =1 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 6 Ω		8	20	ns
Rise Time	tr			10	25	
Turn-Off Delay Time	td(off)			35	70	
Fall-Time	tf			30	60	
Total Gate Charge	Q <sub>g</sub>			10	15	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6A		2.3		nc
Gate-Drain Charge	Q <sub>gd</sub>			2.9		

1、Pulse width limited by Max. junction temperature.

2、Pulse width <300us , duty cycle <2%.

3、Surface Mounted on FR4 Board, t < 10 sec.

## Typical Performance Characteristics

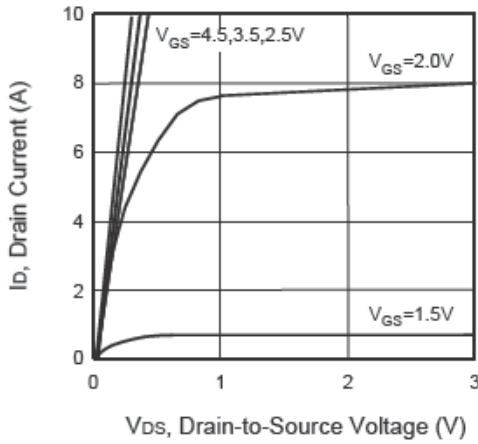


Figure 1. Output Characteristics

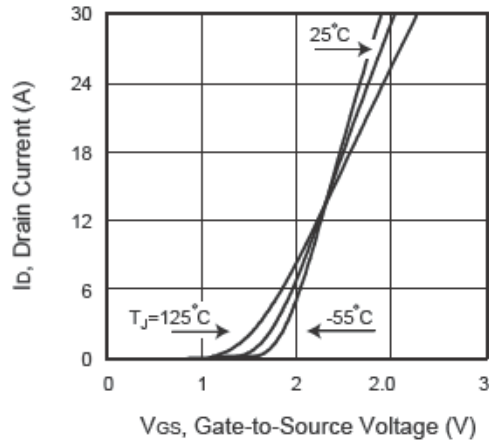


Figure 2. Transfer Characteristics

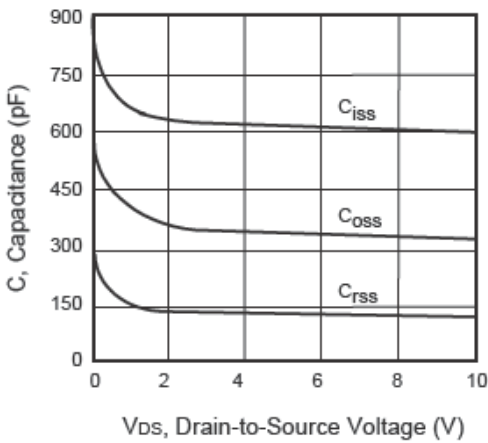


Figure 3. Capacitance

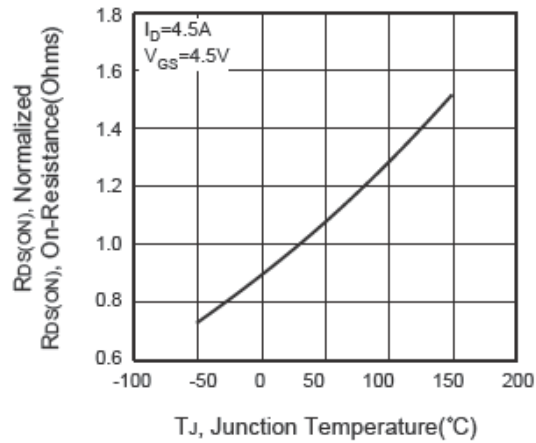


Figure 4. On-Resistance Variation with Temperature

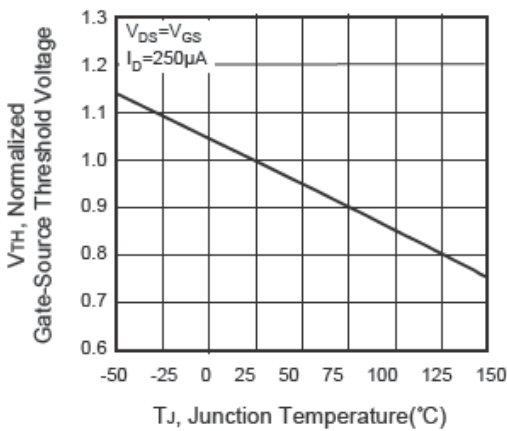


Figure 5. Gate Threshold Variation with Temperature

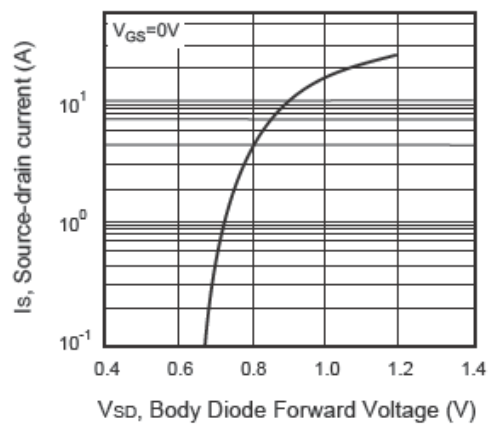


Figure 6. Body Diode Forward Voltage Variation with Source Current

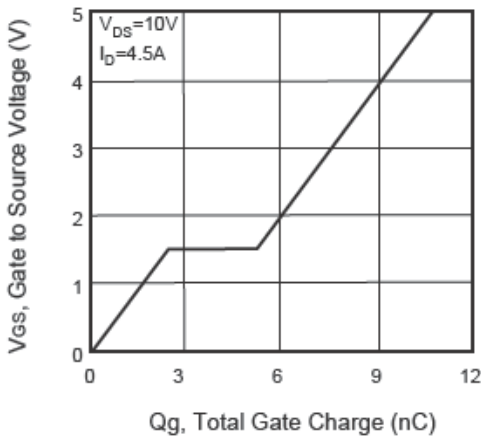


Figure 7. Gate Charge

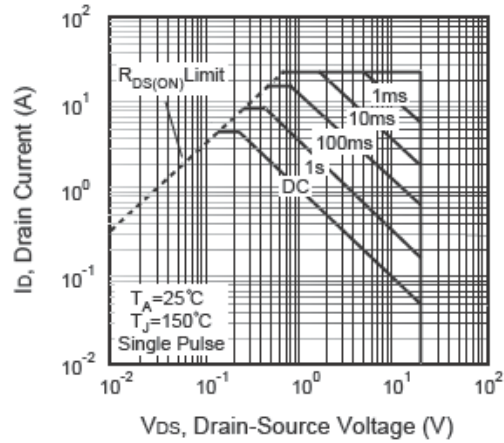


Figure 8. Maximum Safe Operating Area

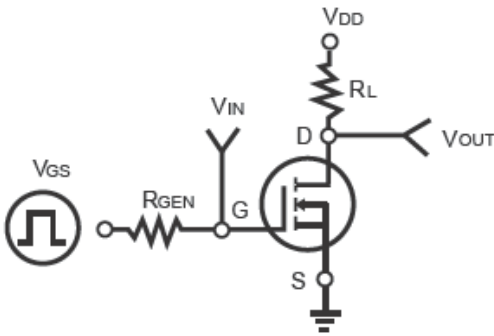


Figure 9. Switching Test Circuit

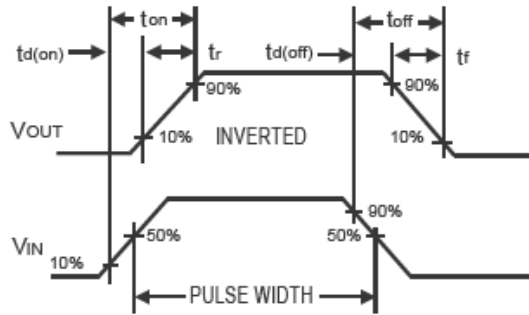


Figure 10. Switching Waveforms

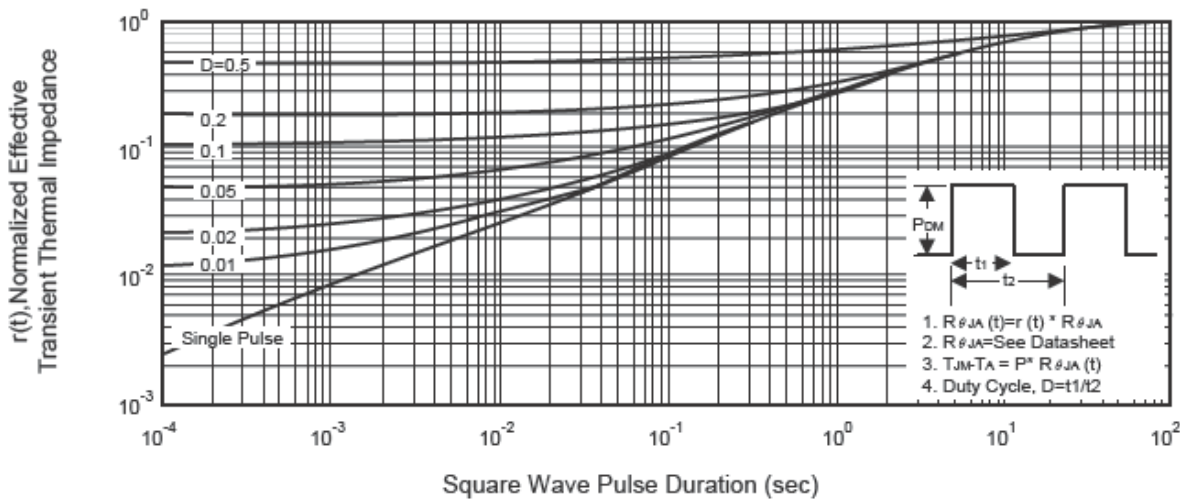
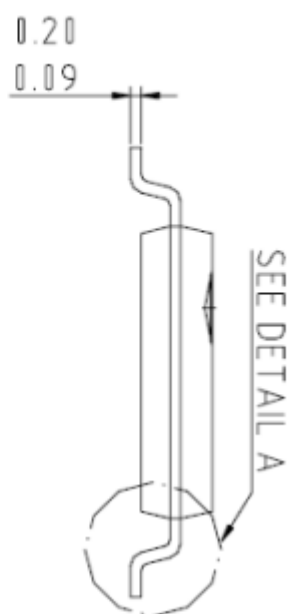
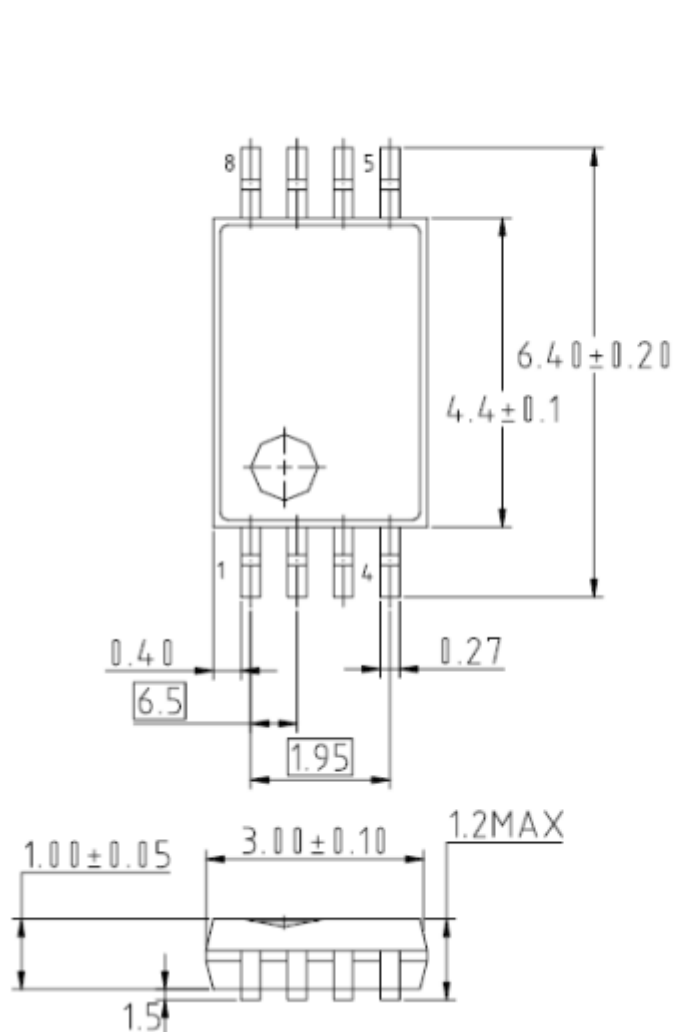


Figure 11. Normalized Thermal Transient Impedance Curve

## Package Information



TSSOP8  
Unit:mm

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