No.	History	Version	Owner
1	First Issue	1.0	Kerven

Signature

QA：	Date：
AE：	Date：
FAE：	Date：
PD：	Date：
R&D：	Date：
Market：	Date：
GM：	Date：

General Description

The MST1530 provides complete Li+ charger protection against input over-voltage, input over-current and thermal shutdown protection is also available. When any of the monitored parameters is over the threshold, the IC turns off the charging current. All protections also have deglitch time against false triggering due to voltage spikes or current transients. The system is positive over-voltage protected up to +30V. Thanks to a very low current consumption, the USB charge is compatible with this integrated component.

The MST1530 provides complete Li+ charger protections, and saves the external MOSFET and Schottky diode for the charger of cell phone's PMIC. This device uses internal PMOS FET, making external devices unnecessary, which reduces the system cost and PCB area of the application board. The above features and small package make the MST1530 an ideal part for cell phones applications. MST1530 is able to instantaneously disconnect the output from the input if the input voltage exceeds the over-voltage threshold. Additional over-current protection function allows turning off internal PMOS FET when the charge current exceeds current limit, which is externally selectable.

The current limit value can be modified with control logic pin to divide it by internal gain, allowing USB 100mA/500mA charging or USB/Wall adapter charging up to over-current threshold. At the same time, Li-ion battery voltage is continuously monitored, providing more safety during the charge.

MST1530 provides a negative going flag (FLAG) output, which alerts the system that a fault has occurred as over-voltage, over-current or thermal event.

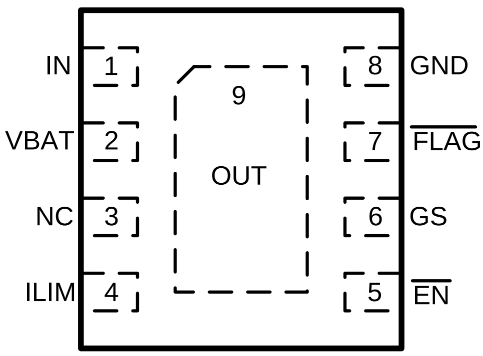
Features

- Over-voltage protection up to +30V
- Fast turn off time
- Very low current consumption/USB compliant
- Li-ion battery voltage monitoring
- Over-voltage lockout (OVLO)
- Under-voltage lockout (UVLO)
- Over-current protection externally adjustable (OCP) up to 2.8A
- Thermal shutdown
- Shutdown $\overline{EN}$ and gain input pins
- Soft start to eliminate inrush current
- Alert $\overline{FLAG}$ output
- Compliance to IEC61000-4-2 (Level 4) 8KV (Contact), 15KV (Air) bypassed with a 1uF or larger capacitor
- ESD Ratings: Machine Model=B
  Human Body Model=2
- 8 Lead DFN 2.2×2mm package
- Pb-free devices

Applications

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Applications
- MP3 Players

Pin Configuration



DFN-8

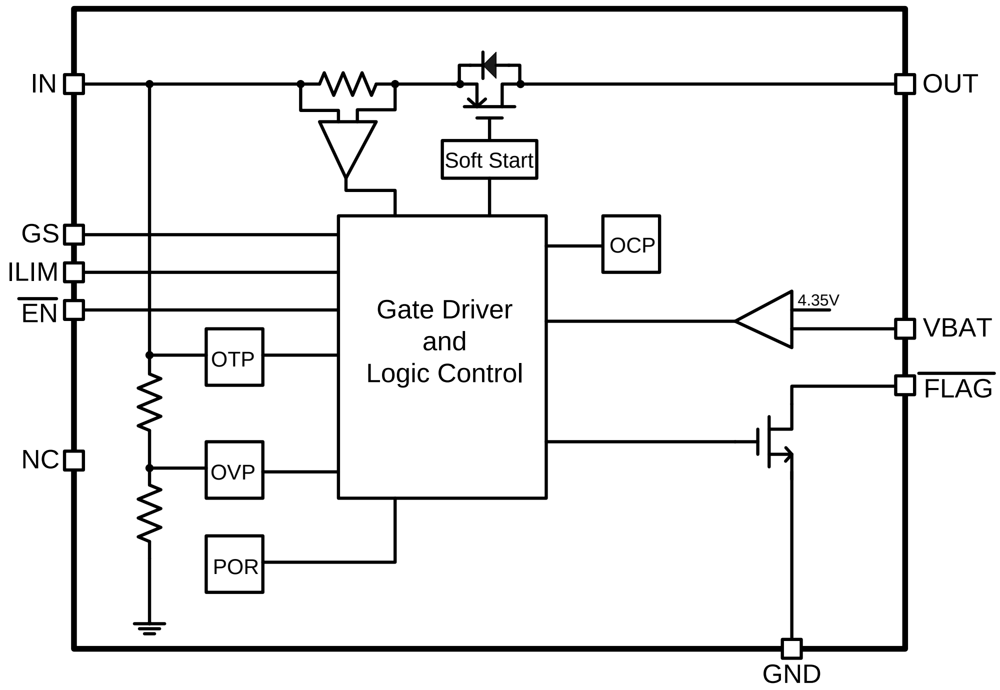
Top View

Pin Descriptions

Pin No.	Pin Name	I/O	Pin Description
1	IN	P	Input voltage pin. A 1uF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
2	VBAT	I	Li-ion battery voltage sense pin.
3	NC	--	No connect
4	ILIM	O	Current limit pin to limit the over-current.
5	$\overline{\text{EN}}$	I	Enable mode pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the pin. The state of this pin does not have an impact on the fault detection of the $\overline{\text{FLAG}}$ pin.
6	GS	I	Gain select pin. When the GS pin is tied to 0 level, the over-current threshold is defined by ILIM setting. When GS pin is tied to high, the over-current threshold is set to ILIM/GS.
7	$\overline{\text{FLAG}}$	O	Fault indication pin. This pin allows an external system to detect fault

			condition. An external pull-up resistor to VBAT must be added(10K Ω minimum value).
8	GND	P	Ground
9	OUT	O	Output voltage pin. This pin follows IN pin when "no input fault" is detected. A 1uF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.

■ Function Block Diagram



■ Absolute Maximum Ratings(Note 1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
IN	Power supply voltage	-0.3	30	V
	All others pin voltage to GND	-0.3	7.0	V
I_{IN}	Maximum DC current from IN to OUT	--	3.4	A
V_{HBM}	Human body model, model=2		2	KV
V_{MM}	Machine model, model=B		200	V
LU	Latchup		Class 1	
MSL	Moisture Sensitivity		Level 1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Air (without PCB area)		190	℃/W
T_A	Operating temperature range	-40	85	℃
T_S	Storage temperature range	-65	150	℃
T_J	Junction operating temperature	--	150	℃

Note1: Exceeding these ratings may damage the device.

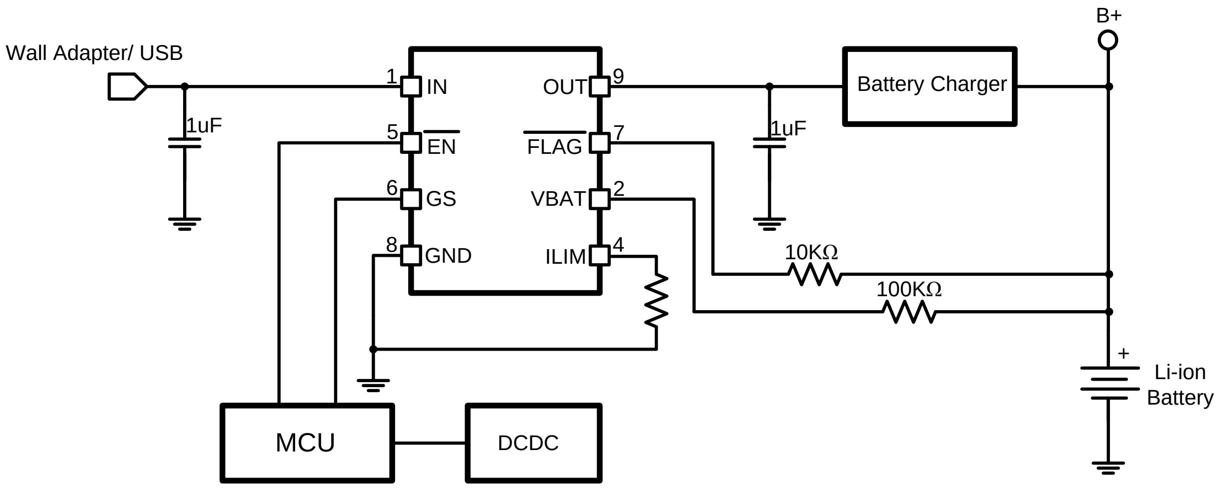
■ Electrical Characteristics

(Min/Max limits values (-40℃<T_A<+85℃) and Vin=+5.0V. Typical values are T_A=+25℃, unless otherwise noted.)

SYMBOL	ITEMS	CONDITIONS	Min.	Typ.	Max.	UNIT
Vin	Input Voltage Range		1.2		28	V
UVLO	Undervoltage Lockout Threshold	Vin falls down UVLO threshold	1.75	1.85	1.9	V
UVLO_hyst	Undervoltage Lockout Hysteresis			80	100	mV
OVLO	Overvoltage Lockout Threshold	Vin rises up OVLO threshold	6.90	7.20	7.50	V
OVLO_hyst	Overvoltage Lockout Hysteresis			100	150	mV
$R_{DS(ON)}$	Vin versus Vout Resistance	Vin=5V, enable mode, load connected to Vout		50	100	mΩ
Idd	Supply Quiescent Current	No load		42	130	uA
Idd_dis	Disable Mode	$\overline{EN}$=1.2V		40	110	uA
I_{OCP}	Overcurrent Threshold	Vin=5V, $\overline{EN}$=low, load connected to Vout, R_{ILIM}=0Ω, 1A/us, GS=0.4V	2.30	2.85	3.40	A
Ireg	Overcurrent Response	1A/us, GS=low, I_{LIM}=1.51A		5.0		%
GS	Current Limit Gain	GS=1.2V		2.55		
OV_{BAT}	Battery Overvoltage Threshold	0℃ to 85℃	4.3	4.35	4.4	V
OV_{HYS}	Battery Overvoltage Hysteresis	0℃ to 85℃	100	150	200	mV
$VBAT_{LEAK}$	VBAT Pin Leakage				20	nA
$VBAT_{DEG}$	VBAT Deglitch Time	VBAT>OV_{BAT}	0.2	2.0	4.0	ms
Vol_{flag}	FLAG Output Low Voltage	Vin>OVLO, sink 1mA on FLAG pin			400	mV
$\overline{FLAG}_{leak}$	FLAG Leakage Current	$\overline{FLAG}$ level=5V		10		nA
Vih	$\overline{EN}$ Voltage High	Vin from 3.3V to 5.25V	1.2			V
Vil	$\overline{EN}$ Voltage Low	Vin from 3.3V to 5.25V			0.4	V
$\overline{EN}_{leak}$	EN Leakage Current	$\overline{EN}$=5.5V or GND		200		nA
Vih	GS Voltage High	Vin from 3.3V to 5.25V	1.2			V
Vil	GS Voltage Low	Vin from 3.3V to 5.25V			0.4	V
GS_{leak}	GS Leakage Current	$\overline{EN}$=5.5V or GND		200		nA
TIMINGS						
t_{on}	Start Up Delay	From Vin>UVLO to Vout=0.8×Vin	15	30	45	ms
t_{start}	FLAG Going Up Delay	From Vout>0.2×Vin to $\overline{FLAG}$=1.2V	15	30	45	ms
t_{REARM}	Rearming Delay	OCP active	15	30	45	ms
t_{REG}	Overcurrent Regulation Time	OCP active	1.2	1.8	3.0	ms
t_{off}	Output Turn Off Time	From Vin>OVLO to Vout≤0.3V, Vin increasing from 5V to 8V at 3V/us		1.5	5.0	us
t_{stop}	Alert Delay	From Vin>OVLO to $\overline{FLAG}$ ≤0.4V, Vin increasing from 5V to 8V at 3V/us		1.5		us
t_{dis}	Disable Time	From $\overline{EN}$ 0.4 to 1.2V to Vout≤0.3V		3.0		us

TIMINGS						
T_{sd}	Thermal Shutdown Temperature			150		℃
T_{sd_hyst}	Thermal Shutdown Hysteresis			30		℃

■ Typical Application Circuit



NOTE: This circuit is for reference only.

■ Operation Description

◆ Operation

The MST1530 is an integrated IC which offers a complete protection of the portable devices during the Li-ion battery charge.

First, the input pin is protected up to +30V, protecting the down stream system (charger, transceiver, system…) against the power supply transients such as inrush current or defective functionality. Additional protection level is offered with the over-current block which eliminates current peak or opens the charge path if an over-current default appears.

More of that, the battery voltage is monitored all along the input power supply is connected, allowing to open charge path if Li-ion battery voltage exceeds 4.3V, caused by CCCV charger or battery pack fault.

The integrated pass element (PMOS FET) is sized to support very high charge DC current up to 2.3A. The over-current threshold can be externally adjusted with a pull-down resistor and gain select pin is available to divide current limit threshold with internal fixed gain. Allowing to adjust with logic pin the over-current threshold if USB/500mA or WA/1.5A is detected, without changing R_{ILIM} resistor, in example.

Under-voltage, over-voltage, over-current and thermal faults are signalized thanks to the open drain $\overline{\text{FLAG}}$ pin, by pulling its down.

◆ Under-voltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built-in under-voltage lockout (UVLO) circuit. During Vin positive going slope, the output remains disconnected from input until Vin voltage is above 1.85V plus hysteresis nominal. This circuit has a 80mV hysteresis to provide noise immunity to transient condition.

- **Over-voltage Lockout (OVLO)**

To project connected systems on Vout pin from over-voltage, the device has a built-in over-voltage lock out (OVLO) circuit. During over-voltage condition, the output remains disabled as long as the input voltage exceeds this threshold.

$\overline{FLAG}$ output is tied to low as long as Vin is higher than OVLO. This circuit has a 100mV hysteresis to provide noise immunity to transient conditions.

- **$\overline{FLAG}$ Output**

MST1530 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon as the OVLO, OV_{BAT}, I_{OCP} or internal temperature thresholds are exceeded and remains low until between minimum driving voltage and UVLO threshold. When Vin level recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1MΩ -minimum 10KΩ) must be provided to Vcc. $\overline{FLAG}$ pin is an open drain output, which is able to support 1mA maximum.

- **$\overline{EN}$ Input**

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. $\overline{EN}$ does not over-drive a UVLO or OVLO fault.

- **Over-current Protection (OCP)**

This device integrates the over-current protection function, from wall adapter to battery. That means the current across the internal PMOS is regulated and cut when the value, set by external R_{SEL} resistor, exceeds I_{LIM} longer than t_{REG}.
An internal resistor is placed in series with the pin allowing to have a maximum OCP value when I_{LIM} pin is directly connected to GND.
By adding external resistors in series with I_{LIM} and GND, the OCP value is decreased.
An additional logic pin, GS (gain select), is very useful in case of different charge rate is necessary (Wall adapter and USB, for example).
By setting GS to 0.4V, over-current thresholds are depending on R select resistor, which is connect between pin 4 and GND. When the GS pin is tied to 1.2V (high logic level) the preselected current limit is divided by 2.55. Thanks to this option, both fast charge or USB charge are authorized with the same device.

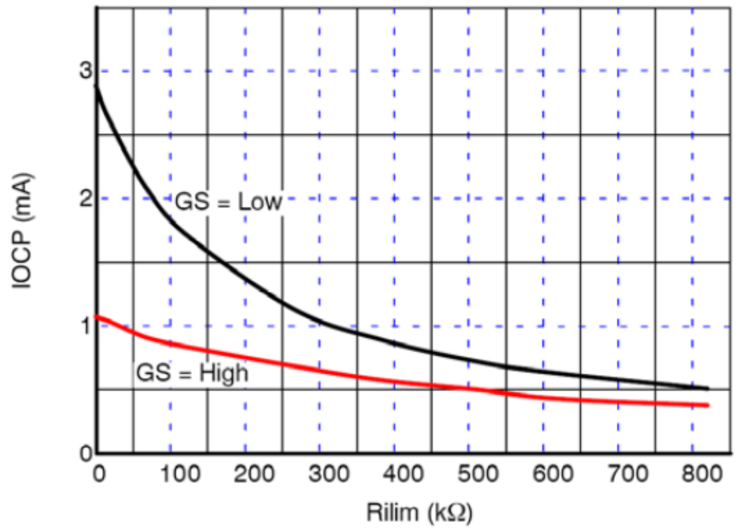


Figure 1. Over-current Threshold vs. R_{ILIM} 2.85A Version

Typical R_{ILIM} calculation is following:

R_{ILIM} (KΩ)=532/I_{OCP}-180

During over-current event, charge area is opened and $\overline{FLAG}$ output is tied to low, allowing the controller to take into account the fault event and then open the charge path.

At power up (accessory is plugged on input pins), the current is limited up to I_{LIM} during 1.8ms (typical), to allow capacitor charge and limit inrush current. If the I_{LIM} threshold is exceeded over 1.8ms, the device enter in OCP burst mode until the over-current event disappears.

- **VBAT Sense**

The connection of the VBAT pin to the positive connection of the Li-ion battery pack allows preventing over-voltage transient, greater than 4.35V. In case of wrong charger conditions, the PMOS is then opened, eliminating battery pack over voltage which could create safety issues and temperature increasing.

The 4.35V comparator has a 150mV built-in hysteresis.

More of that, deglitch function of 2ms is integrated to prevent voltage transients on the battery voltage.

If the battery over voltage condition exceeds deglitch time, the charge path is opened and $\overline{FLAG}$ pin is tied to low level until the VBAT is greater than 4.35V hysteresis.

At wall adapter insertion, and if the battery is fully charged, VBAT comparator stays locked until battery needs to be recharged (4.2V typ.-4.1V min).

A serial resistor has to be placed in series with VBAT pin and battery connection, with a 200KΩ recommended value.

- **PCB Recommendations**

The MST1530 integrated low $R_{DS(ON)}$ PMOS FET, nevertheless PCB layout rules must be respected to properly evacuate the heat out of the silicon. The DFN PAD1 corresponds to the PMOS drain so must be connected to OUT plane to increase the heat transfer. Of course, in any case, this pad shall be not connected to any other potential.

Following figure shows package thermal resistance of a DFN 2.2×2 mm.

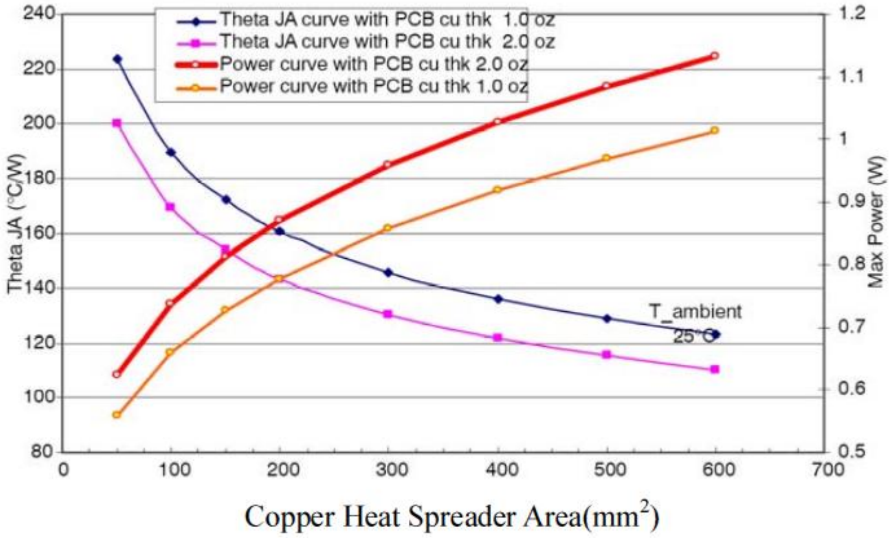


Figure 2. DFN Package Thermal Resistance

- **Internal PMOS FET**

MST1530 includes an internal PMOS FET to protect the system, connected on OUT pin, from positive over-voltage. Regarding electrical characteristics, the $R_{DS(ON)}$, during normal operation, will create low losses on VOUT pin versus Vin, thanks to very low $R_{DS(ON)}$.

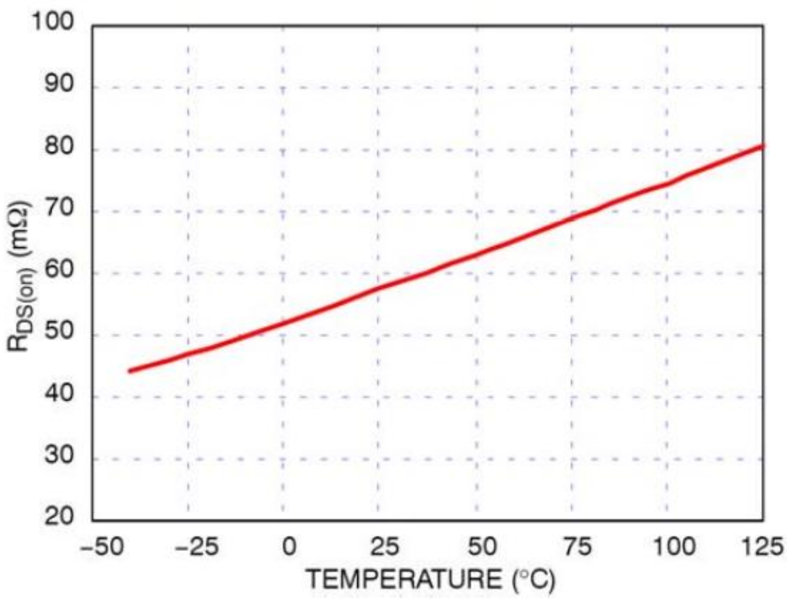


Figure 3. Typical $R_{DS(ON)}$ versus Temperature

- **ESD Tests**

MST1530 fully support the IEC61000-4-2, level 4 (Input pin, 1uF mounted on board). That means, in Air condition, Vin has a ±15KV ESD protected input. In Contact condition, Vin has ±8KV ESD protected input. Please refer to Figure 4 to see the IEC61000-4-2 electrostatic waveform.

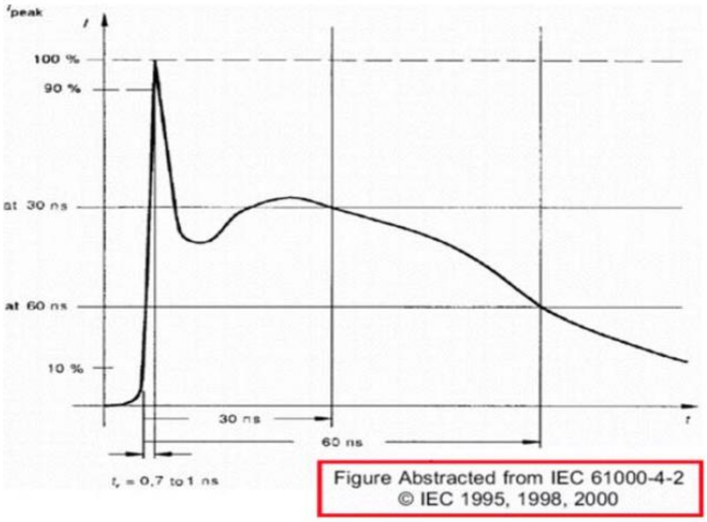


Figure 4. IEC61000-4-2 Electrostatic Discharge

■ Typical Operating Characteristics

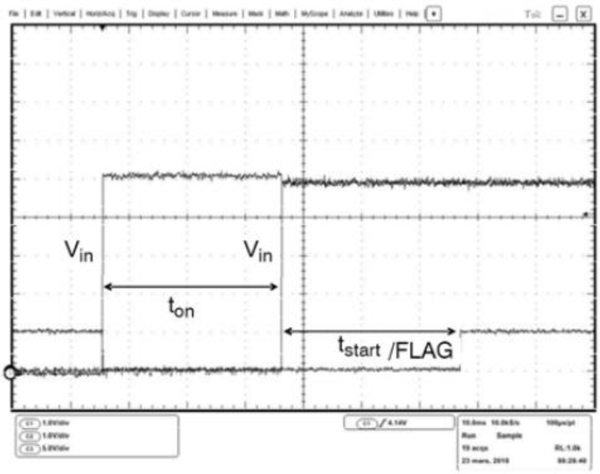


Figure 5. Hot Plug-in from 0V to 5V, t_{on} and t_{start}

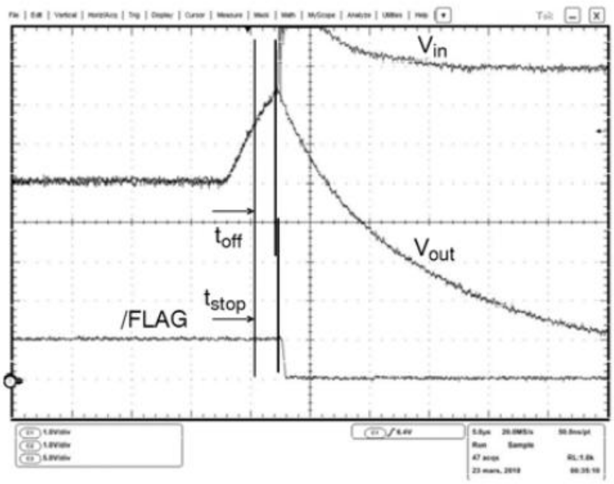


Figure 6. Over-voltage from 5V to 8V, t_{off} and t_{stop}

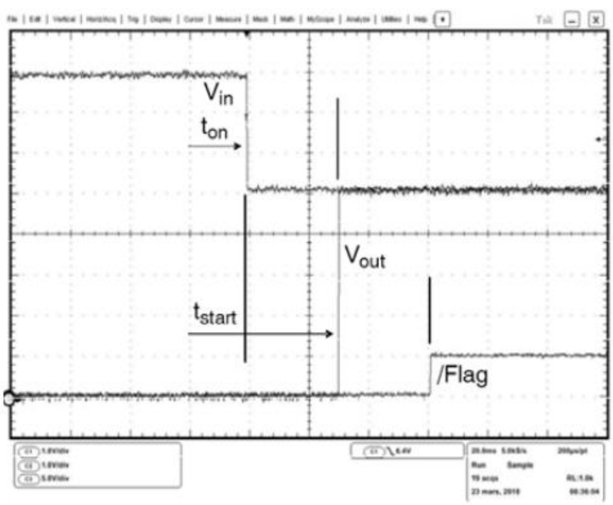


Figure 7. Retrieve Normal Operation, t_{on} and t_{start}

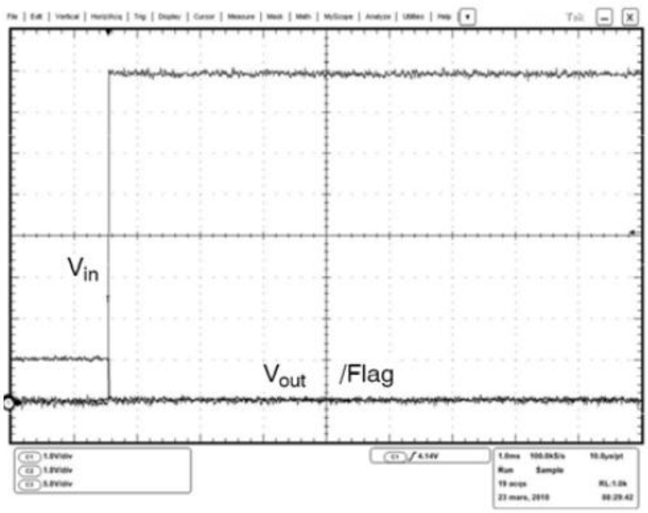


Figure 8. Over-voltage from 0V to 10V

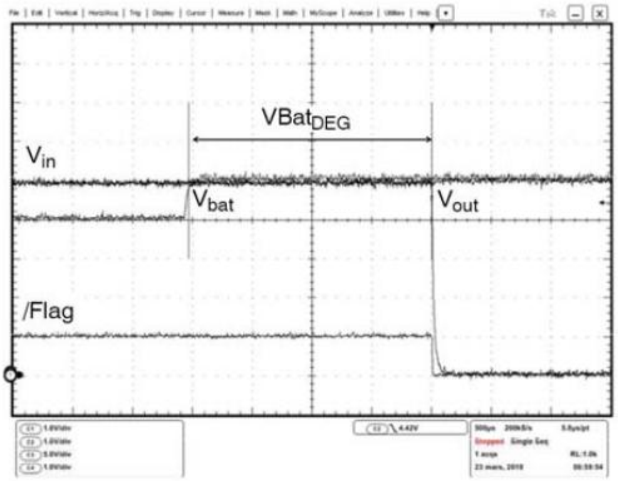


Figure 9. Battery Over-voltage, Deglitch Time

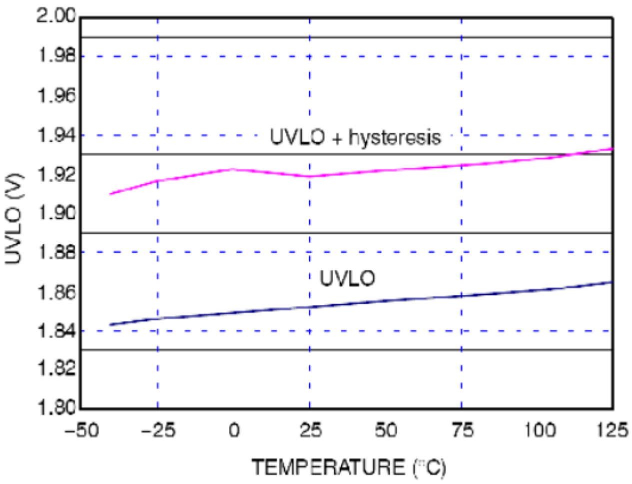
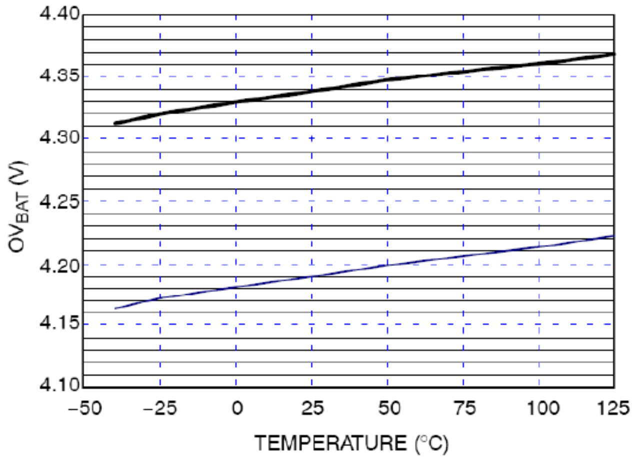


Figure 10. UVLO and Hysteresis



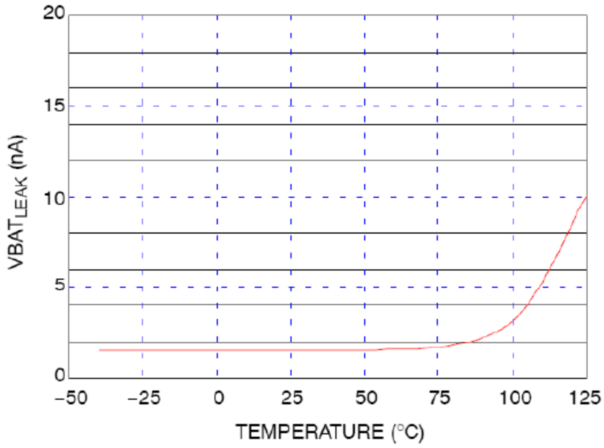


Figure 11. VBAT Threshold and Hysteresis vs. Temperature Figure12.VBAT Pin Leakage vs. Temperature

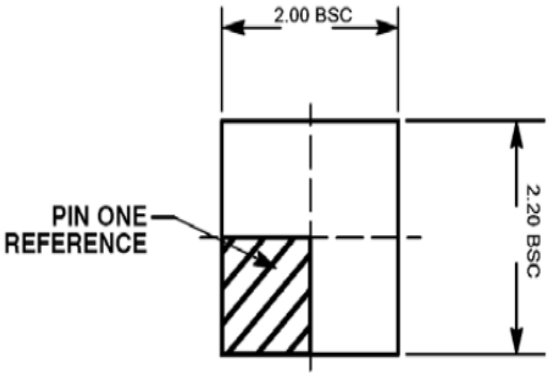
■ Ordering Information

Part Number	Package	Marking
MST1530SF	DFN-8	CEY①W②X③

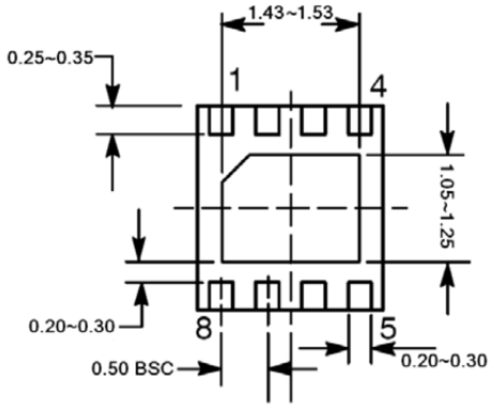
Remark: ①Y=Production Year, for example (5=2015)
②W=Production Week, for example (A=first week, B=second week, a=twenty-seventh week)
③X=Internal identification number

■ **Package Outlines**

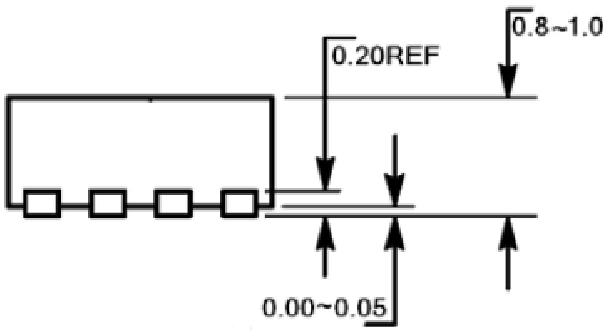
DFN-8



Top view

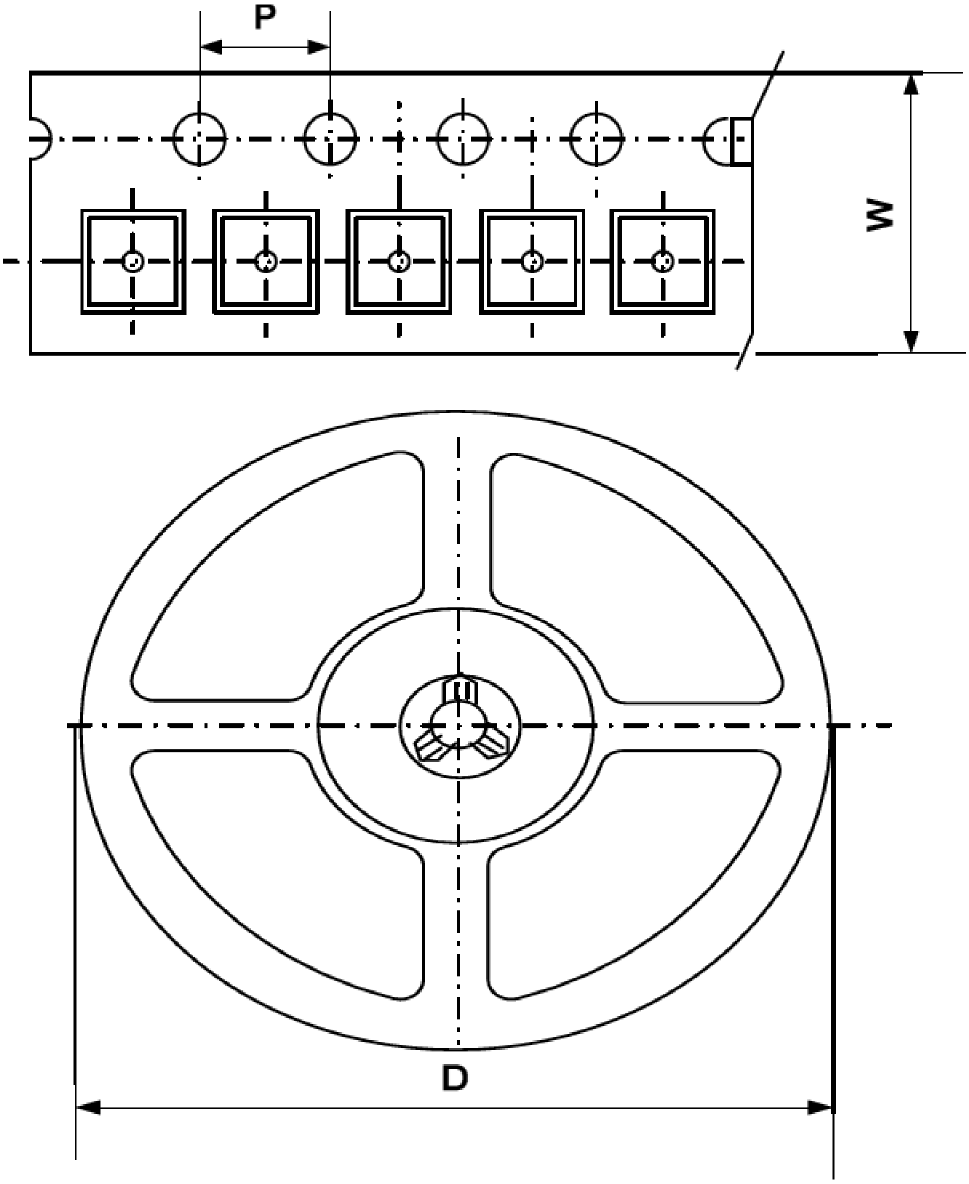


Bottom view



Side view

■ Packing Information



Package Type	Carrier Width (W)	Pitch (P)	Reel Size(D)	Packing Minimum
DFN-8	12.0±0.1 mm	8.0±0.1 mm	330±1 mm	3000pcs

Note: Carrier Tape Dimension, Reel Size and Packing Minimum is for reference only.