4A,34V High Efficiency Synchronous Step-Down DC/DC Converter

Description

NDP1340KC is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. Capable of delivering up to 4A continuous load with excellent line and load regulation. The device operates from an input voltage range of 6.5V to 32V and provides an adjustable output voltage from 1V to 25V.

The NDP1340KC features short circuit and thermal protection circuits to increase system reliability. The internal soft-start avoids input inrush current during startup.

The NDP1340KC require a minimum number of external components. and a wide array of protection features to enhance reliability

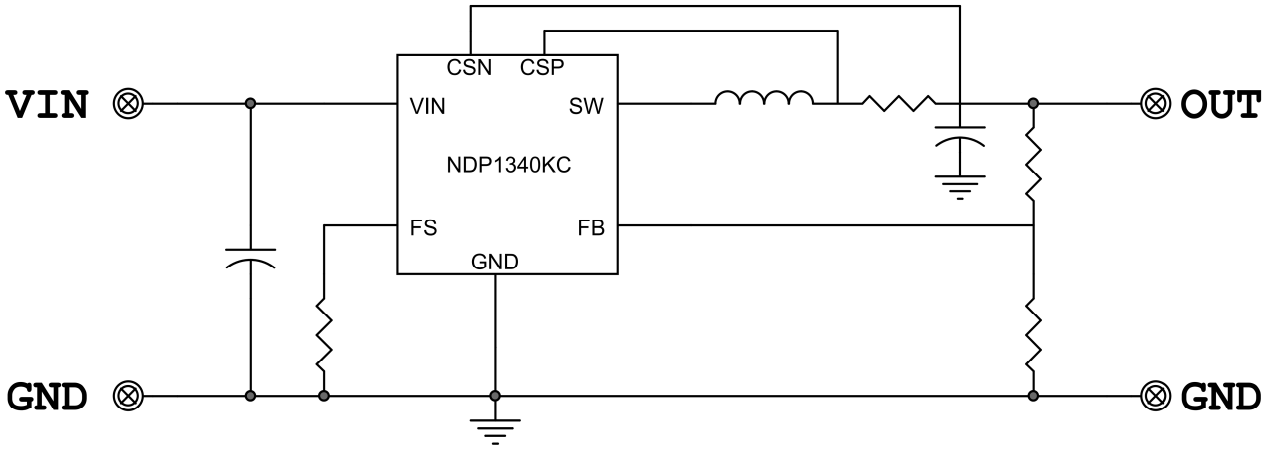
Features

- Wide VIN Range : 6.5V to 32V
- 4A Continuous Output Current
- Up to 94% I Efficiency
- CC/CV Mode Control
- 100% Max Duty Cycle
- Built in Adjustable Cable Drop Compensation
- Cable drop Compensation up to 2.0V
- Adjustable Output Voltages
- +/-1.5% Output Voltage Accuracy
- +- 5% Current Limit Accuracy.
- Integrated 38mΩ High Side Switch
- Integrated 18mΩ Low Side Switch
- Programable Frequency(130KHz~300KHz)
- Burst Mode Operation at Light Load
- Internal loop Compensation
- Internal Soft Start
- Available in SOP8 Package

Applications

- Car Charger
- Rechargeable Portable Devices
- Networking Systems
- Distributed Power Systems

Typical Application



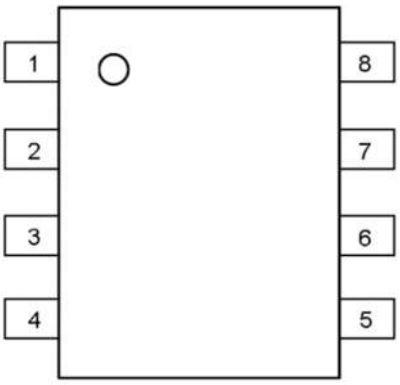
Note: When using a solid or ceramic input Cap, It is recommended to parallel a TVS diode.

Absolute Maximum Ratings (at TA = 25°C)

Characteristics	Symbol	Rating	Unit
VIN to GND		-0.3 to 34	V
SW to GND		-0.3 to VIN+0.3	V
FB, FS to GND		-0.3 to +6	V
CSP, CSN to GND		-0.3 to 25	V
Junction to Ambient Thermal Resistance		105	°C/W
Operating Junction Temperature		-40 to 150	°C
Storage Junction Temperature		-55 to 150	°C
Thermal Resistance from Junction to case	θ_{JC}	15	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	40	°C/W

Pin Function And Descriptions

PIN	NAME	Description
1	VFB	Feedback Of Output Voltage
2	CSP	Positive Pole of Current Sense
3	CSN	Negative Pole1 of Current Sense
4	VIN	Power Input Positive Pole
5,6	SW	Switching, Connected With a Inductor
7	FS	Connect a Resistor to GND for Frequency Config
8	GND	Ground



Order information

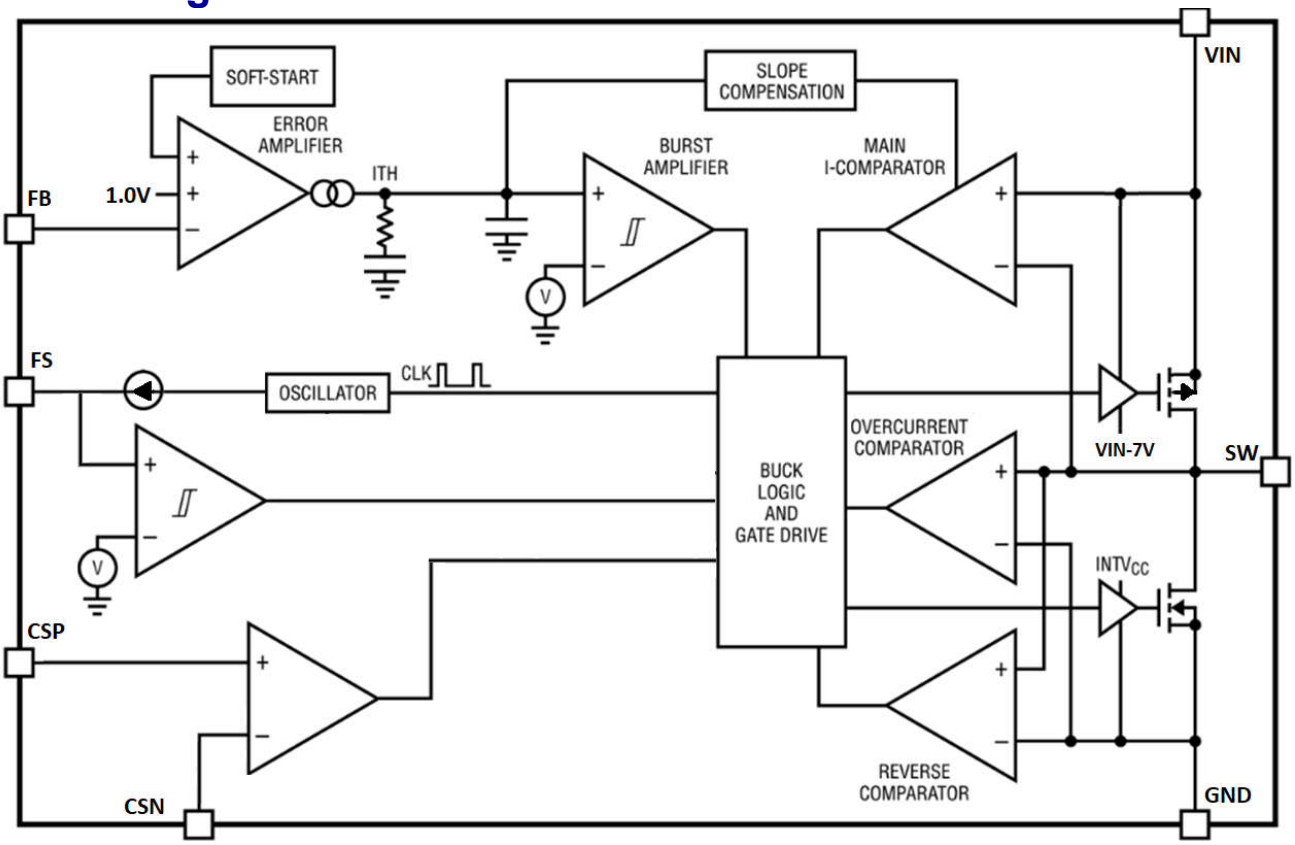
Order Information	Top Marking
NDP1340 K C Pin NO. C:8 Package K: SOP Product Number	 DY: Year (D8=2018,D9=2019,…) WW: Weekly (01-53) X : Internal ID Code

Electrical Characteristics

TJ = 25°C. VIN = 12V, unless otherwise noted

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	VIN		6.5	-	32	V
UVLO Voltage	V_{UVLO}		5	5.5	6	V
UVLO Hysteresis			0.3	0.5	0.8	V
Input over voltage protect	Vovp		32			V
Quiescent Current	I_{CCQ}	V_{FB} = 1.2V, no switch	-	1300	-	uA
Standby Current	I_{SB}	No Load	-	1.7	2.2	mA
FB Reference Voltage	V_{FB}		0.985	1	1.015	V
V_{FB} bias Current	I_{FB}				0.2	uA
Current Sense AMP	V_{CS}	CSP-CSN	57	60	63	mV
Switching Frequency	F_{SW}	FS Floating		130		KHz
		connect 470K resister		300		KHz
FS Shut down	V_{FSEN}			0.3	0.4	V
Maximum Duty Cycle				100	-	%
Minimum On-Time			-	250	-	ns
Current Limit	I_{LIM}		4.5			A
VFB short protect	VFB_{SCP}			0.6		V
Hicup Interval	Thiccup			500		mS
Soft start Time	Tss			2		mS
RDS_{ON} Of Power MOS	High side	Temp=25℃			38	mΩ
	Low side	Temp=25℃			18	mΩ
Thermal Regulation	T_{TR}			145		°C
Thermal shutdown Temp	T_{SD}		-	150	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	30	-	°C

Block Diagram



Typical Performance Characteristics (TJ = 25°C, unless otherwise noted)

Operation

The NDP1340KC is a high efficiency, monolithic, synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. Average current mode control enables fast and precise control of the output current. It operates through a wide VIN range and regulates with low quiescent current. An error amplifier compares the output voltage with a internal reference voltage of 1.0V and adjusts the peak inductor current accordingly. overvoltage and undervoltage comparators will turn off the regulator.

Main Control Loop

During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle, causing the inductor current to increase. The sensed inductor current is then delivered to the average current amplifier, whose output is compared with a saw-tooth ramp. When the voltage exceeds the vduty voltage, the PWM comparator trips and turns off the top power MOSFET. After the top power MOSFET turns off, the synchronous power switch (N-channel MOSFET) turns on, causing the inductor current to decrease. The bottom switch stays on until the beginning of the next clock cycle, unless the reverse current limit is reached and the reverse current comparator trips. In closed-loop operation, the average current amplifier creates an average current loop that forces the average sensed current signal to be equal to the internal ITH voltage. Note that the DC gain and compensation of this average current loop is automatically adjusted to maintain an optimum current-loop response. The error amplifier adjusts the ITH voltage by comparing the divided-down output voltage (VFB) with a 1.0V reference voltage. If the load current changes, the error amplifier adjusts the average inductor current as needed to keep the output voltage in regulation.

Low Current operation

The discontinuous-conduction modes (DCMs) are available to control the operation of the NDP1340KC at low currents. Burst Mode operation automatically switch from continuous operation to the Burst Mode operation when the load current is low

VIN Overvoltage Protections

In order to protect the internal power MOSFET devices against transient voltage spikes, the NDP1340KC constantly monitors the VIN pin for an overvoltage condition. When VIN rises above 32V, the regulator suspends operation by shutting off both power MOSFETs. Once VIN drops below 31.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Cable Drop Compensation

Due to the resistive of charger's output Cable, The NDP1340KC built in a simple user programmable cable voltage drop compensation using the impedance at the FB pin. Choose the proper resistance values for charger's output cable as show in table 1:

R_{up} is the upper resistor the resistors divider net

R_{low} is the lower resistor the resistors divider net

$R_{FB(UPER)}$（K）	R_{low}（K）	Cable Drop compensation (mV)
100	25	130
160	39	200
360	91	500
470	120	680
820	200	1200
1200	300	1800

table 1

Frequency Selection and Shutdown

The switching frequency of the NDP1340KC can be programmed through an external resistor between 130kHz and 300 kHz，Floating this pin set the switching frequency to 130K, an external resistor can set the frequency up to 300KHz。the switching frequency is set by using the FS pins as shown in Table 2:

FS Resistor(KΩ)	Frequency(KHz)
Floating	130K
2000	180K
1000	220K
510	290K
300	380K
200	470K

When the FS pin is below 0.3V, the NDP1340KC enters a low current shutdown state, reducing the DC supply current to 1.3mA.

Applications Information

Input Capacitor (CIN) Selection

The input capacitance CIN is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at VIN = 2VOUT, where: IRMS ≅ IOUT/2

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (COUT) Selection

The selection of COUT is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, △VOUT, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since △IL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is

important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Copper losses also increase as frequency increases Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coilcraft, Toko, Vishay, NEC/Tokin, TDK and Würth Electronik.

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of IOUT(MAX). To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as: % Efficiency = 100% – (Loss1 + Loss2 + …) where Loss1, Loss2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit

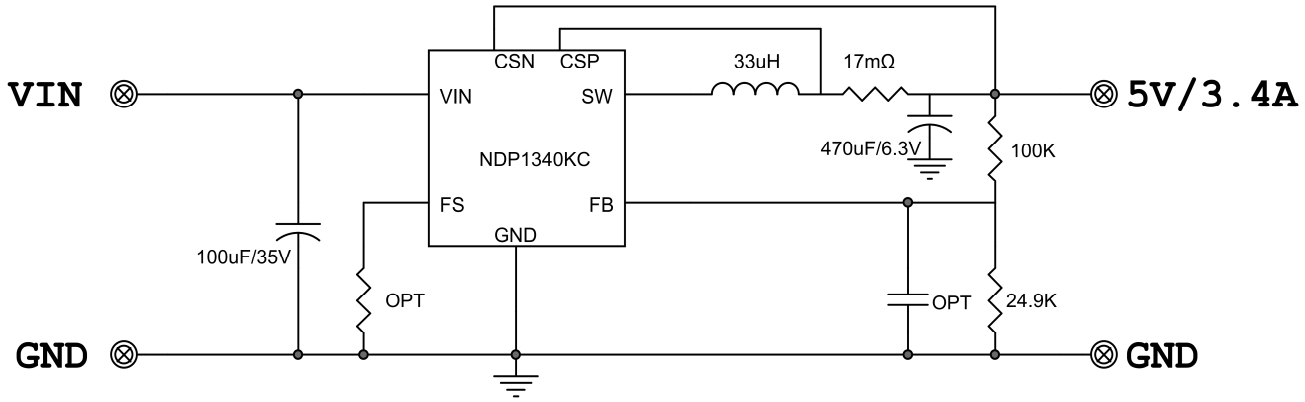
produce losses, three main sources usually account for most of the losses in NDP1340KC circuits: 1) I2R losses, 2) switching and biasing losses, 3) other losses.

Thermal Conditions

In a majority of applications, the NDP1340KC does not dissipate much heat due to its high temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off until the temperature drops about 30°C cooler To avoid the NDP1340KC from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or forced air flow.

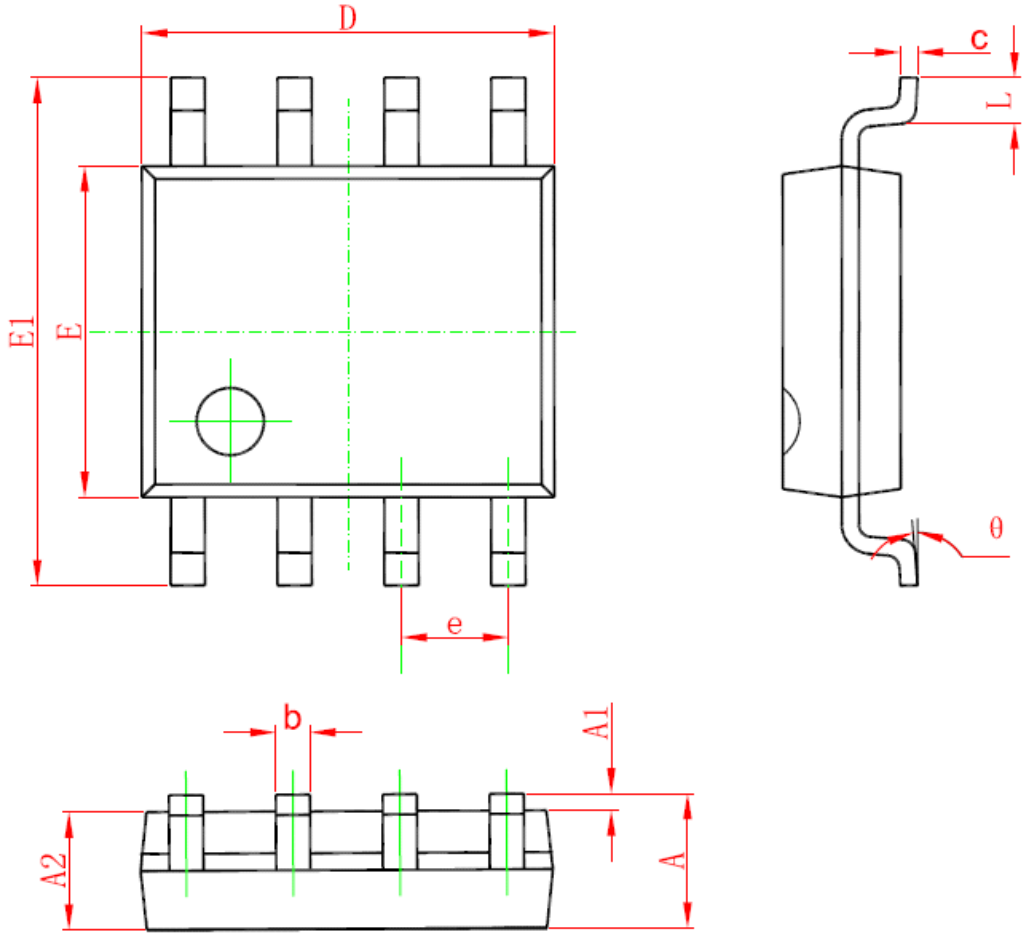
efficiency and low thermal resistance. However, in applications where the NDP1340KC is running at high ambient temperature, high VIN, and maximum output current load, the heat dissipated may exceed the maximum junction

Typical Applications



Package Description

8-Lead Standard Small Outline Package [SOP-8]



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.15	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°